

IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A processor, comprising:

a processor core; and

a memory operatively coupled to said processor core;

wherein said processor core is designed using the method comprising:

selecting a cache size from given candidates;

selecting an instruction memory size from given candidates;

selecting a data memory size from given candidates;

selecting at least one of a plurality of option instructions to be implemented

within said processor core from given candidates.

Claim 2 (Original): The processor according to Claim 1, wherein said option instructions include a dividing option instruction (DIV) and a maximum/minimum value option instruction (MINMAX).

Claim 3 (Original): The processor according to Claim 1, wherein said processor core is provided with an instruction cache and a data cache.

Claim 4 (Currently Amended): The processor according to Claim 1, wherein said cache size, said instruction memory size, said data memory size, and said option instructions are provided in RTL templates accessible by the processor core.

Claim 5 (Currently Amended): The processor according to Claim 1, wherein said method further comprises selecting optional hardware associated with said processor core.

Claim 6 (Currently Amended): A system LSI, comprising:

a processor core;

a memory operatively coupled to said processor core and a user defined module;

wherein said processor core is configured using the method comprising:

selecting a cache size from given candidates;

selecting an instruction memory size from given candidates;

selecting a data memory size from given candidates;

selecting at least one of a plurality of option instructions to be implemented within said processor from given candidates.

Claim 7 (Original): The system LSI according to Claim 6, wherein said option instructions include a dividing option instruction and a maximum/minimum value option instruction.

Claim 8 (Original): The system LSI according to Claim 6, wherein said processor is provided with an instruction cache and a data cache.

Claim 9 (Currently Amended): The system LSI according to Claim 6, wherein said cache size, said instruction memory size, said data memory size, and said option instructions are provided in RTL templates accessible by the processor core.

Claim 10 (Currently Amended): A method of generating a design of a system LSI using a description language, comprising:

preparing a configuration specifying a file including variable item definition information concerning a multiprocessor configuration;
creating a customized description language mode; and
logically composing said design based on said description language model, wherein
said variable item definition information contains at least one item of option instruction
information and information concerning a user defined module and a multiprocessor
configuration.

Claim 11 (Original): The method of Claim 10, wherein said description language
comprises a hardware description language (HDL).